independently from other data memory banks;

wherein said computing devices has at least an integer computing device, and a computing device operating operands including data other than integers.

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3. (Amended) A processor according to claim 1, wherein at least one of said computing devices can execute a data transfer instruction for transferring data between said memory and said register file.

4. (Amended) A processor according to claim 2, wherein at least one of said computing devices can execute a data transfer for transferring data between said memory and said register file.

REMARKS

Claims 1-4 are pending. By this Preliminary Amendment, claims 1-4 are amended.

Substantive of examination, allowance in due course is earnestly solicited..

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

The Office is authorized to charge any fees due under 37 C.F.R. §1.16 or 1.17 to Deposit Account 11-0600.

Should there by any questions concerning this matter, the Examiner is invited to contact the Applicants undersigned attorney.

Respectfully submitted,

KENYON & KENYON

Dated: March 15, 2002

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1-4 as follows:

1. (Amended) A processor, comprising:

a memory for storing an instruction code and data;

an instruction code holding means for holding a plurality of instruction codes read from said memory; and

a plurality of computing units operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

[wherein each computing unit includes a plurality of computing devices and a plurality of access port register files, each of said plurality of computing devices reading a content of each of said register files from a corresponding access port for computation, and said plurality of computing units each having a same function.]

an access port register file being shared by said plurality of computing devices, each of said plurality of computing devices reading/writing a content of said register file through a corresponding access port for computation; and

a plurality of data memory banks each operated with at least one of said computing devices having means for issuing an instruction to load/store data to/from said access port register file,

independently from other data memory banks.

2. (Amended) A processor comprising:

a memory for storing an instruction code and data;

an instruction code holding means for holding a plurality of instruction codes read from said memory; and

a plurality of computing units operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

[wherein each computing unit includes a plurality of computing devices and a plurality of access port register files, each of said plurality of computing devices reading from a corresponding access port for computation, and said plurality of computing units each has a subset of devices having a same function.]

an access port register file being shared by said plurality of computing devices, each of said plurality of computing devices reading/writing a content of said register file through a corresponding access port for computation; and

a plurality of data memory banks each operated with at least one of said computing devices having means for issuing an instruction to load/store data to/from said access port register file, independently from other data memory banks;

wherein said computing devices has at least an integer computing device, and a computing device operating operands including data other than integers.

3. (Amended) A processor according to claim 1, wherein at least one of said computing [device in said computing unit] devices can execute a data transfer instruction for transferring data between said memory and said register file.

4. (Amended) A processor according to claim 2, wherein at least one of said computing [device in said computing unit] devices can execute a data transfer for transferring data between said memory and said register file.